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BT
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Fitzgerald et al. **GROUP:** Unknown

SERIAL NO: 09/884,172 **EXAMINER:** Unknown

FILED: June 19, 2001

FOR: METHOD OF FABRICATING CMOS INVERTER AND
INTEGRATED CIRCUITS UTILIZING STRAINED
SILICON SURFACE CHANNEL MOSFETS

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

In compliance with 37 C.F.R. §§1.56, 1.97, and 1.98, Applicant submits copies of the documents listed on the attached Form PTO-1449. Applicant previously submitted this cited reference incorrectly.

The Commissioner is authorized to charge Deposit Order Account No. 19 0079 for any further fee that is required.

Respectfully submitted,

Matthew E. Connors
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I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited on the date shown below with sufficient postage addressed to the: Commissioner of Patents and Trademarks, Washington, D.C. 20231, Attn: Box IDS

Deborah M. Costello

Date

12/19/01



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